ABSTRACT OF THE DISCLOSURE

In a data transmission circuit according to the present invention, selection circuits alternately switch between transistors of a main buffer and transistors of a dummy buffer. In high-speed data transmission, a H/L transmission switch circuit outputs high-speed data to a constant current driver and outputs a selection signal for inputting a control signal to the main buffer to a selection circuit. In low-speed data transmission, on the other hand, the H/L transmission switch circuit outputs a selection signal for inputting a control signal to the main buffer in accordance with the low-speed data to the selection circuit. The H/L transmission switch circuit controls an input of the control signal to the main buffer in accordance with the selection signal.